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(54) Solid state on-person data carrier and associated data processing system

(57) A pocket-size object which may be used as a 'card' for a variety of personally based data transactions. (personal identification, supply of a control function to a machine, debiting an account with instant (off-line) credit sufficiency check; a method of securely paying to a vending machine, etc, comprises in combination:
magnetically permeable elements; at least one integrated circuit comprising memory and logic functions; ac/dc converting means for providing the internal operating voltages at the moment of use; and means for sequential synchronizing with a fixed data processing installation. The data carrier comprises memory devices which are so constituted that they can hold data after power is removed and in the preferred form a single chip is shown to comprise both memory, address-, logic, and computing functions.

The component also has spare memory capacity reserved for holding a special 'check number' which, however, cannot be read out by any means. They serve the security protection of the main data and provide a safeguard that only authorized alteration of the data contents can take place.

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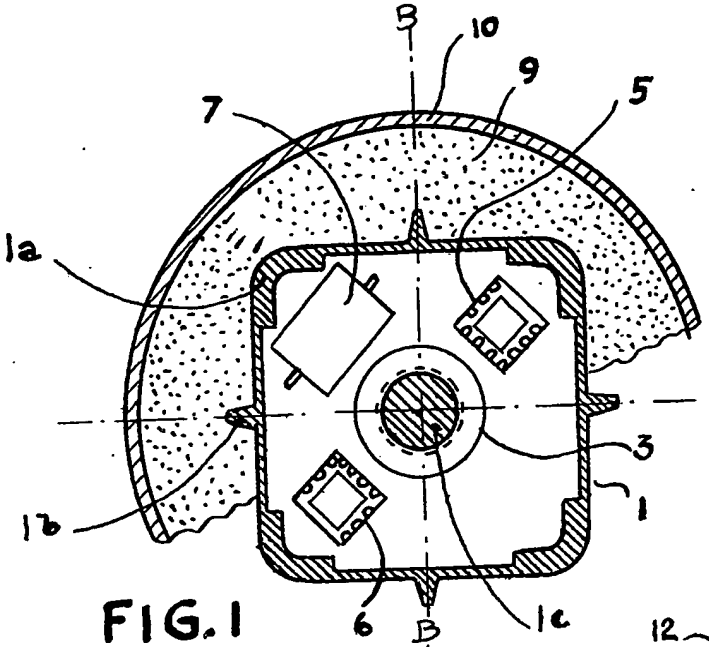

FIG. 1

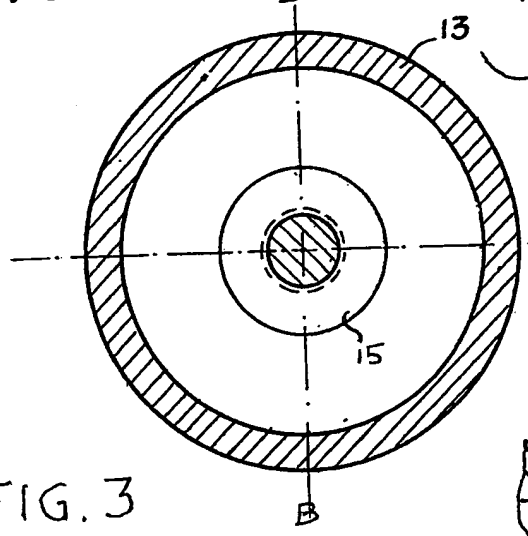

FIG. 3

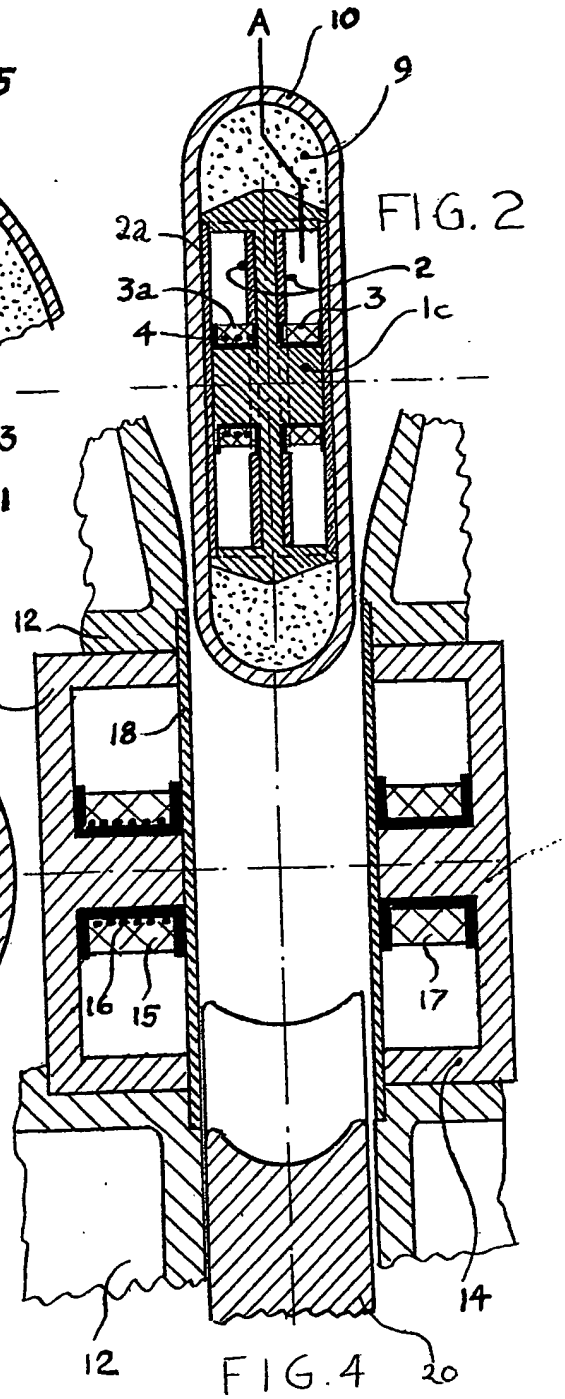

FIG. 2

FIG. 4

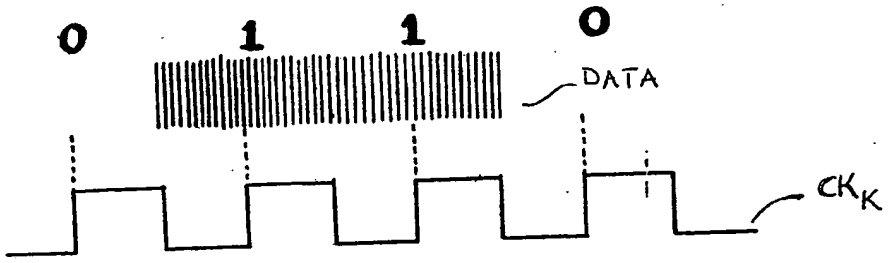

FIG. 5

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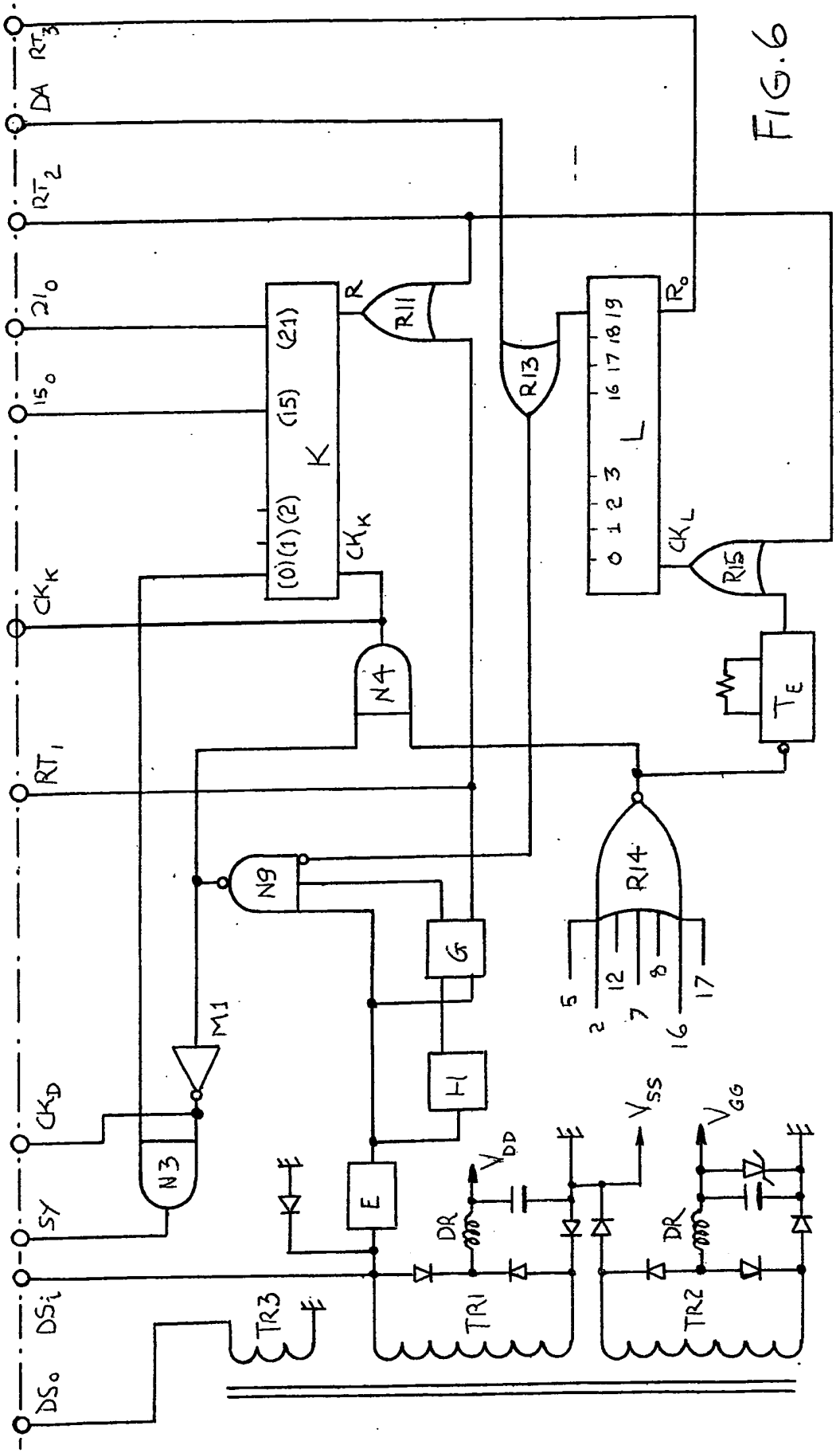

FIG.6

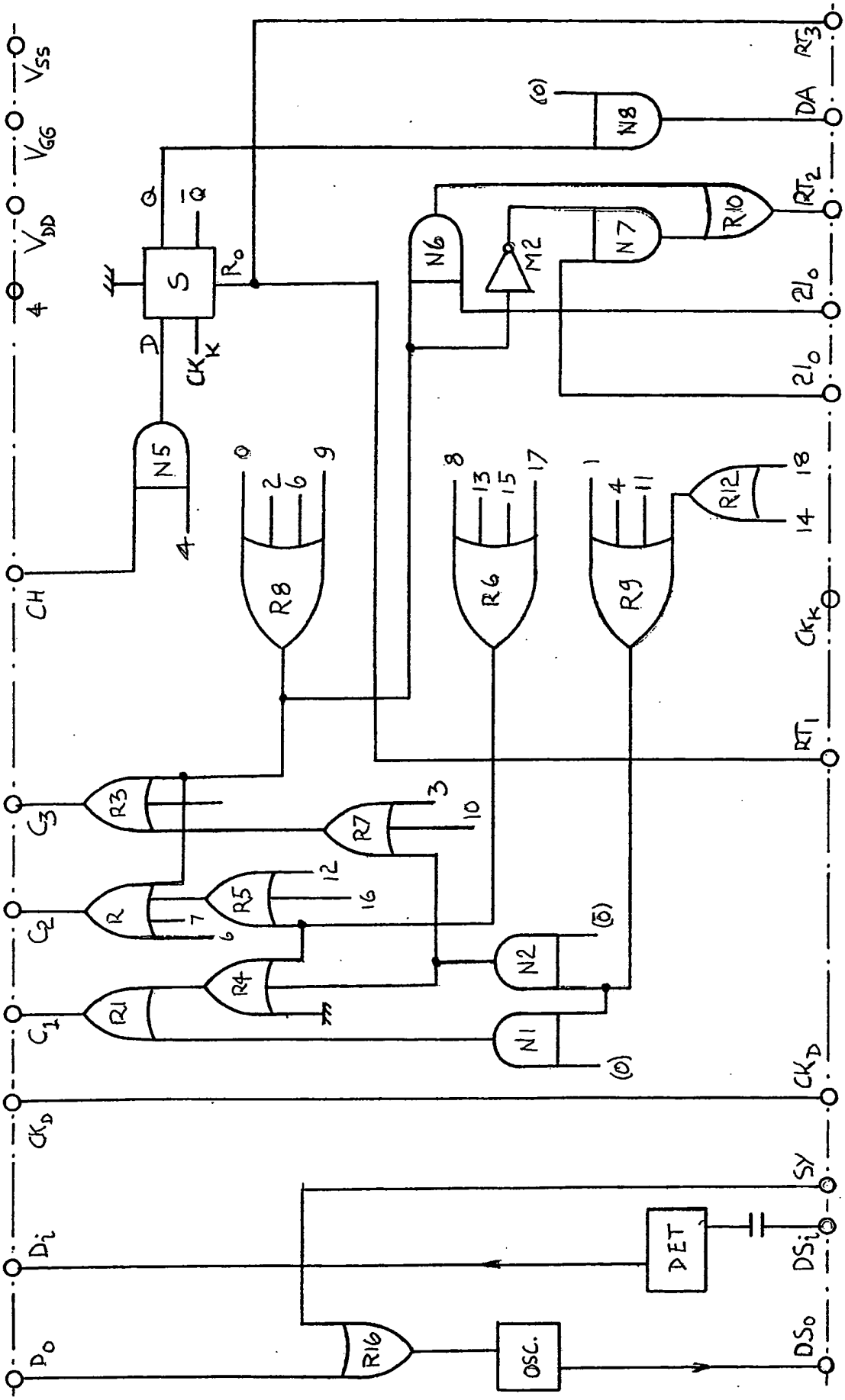
VSS
VGG
VDD
4
CH
N5
S
R
D
CK
Q
Q̄
N8
N6
M2
N7
R10
RT3
DA
RT2
21
21
R8
R6
R9
R12
C3
C2
C1
R3
R7
R
R5
R4
R1
N2
N1
RT1
CKK
CKD
SY
DSi
DET
Di
DSo
R16
OSC.
Do

FIG 7

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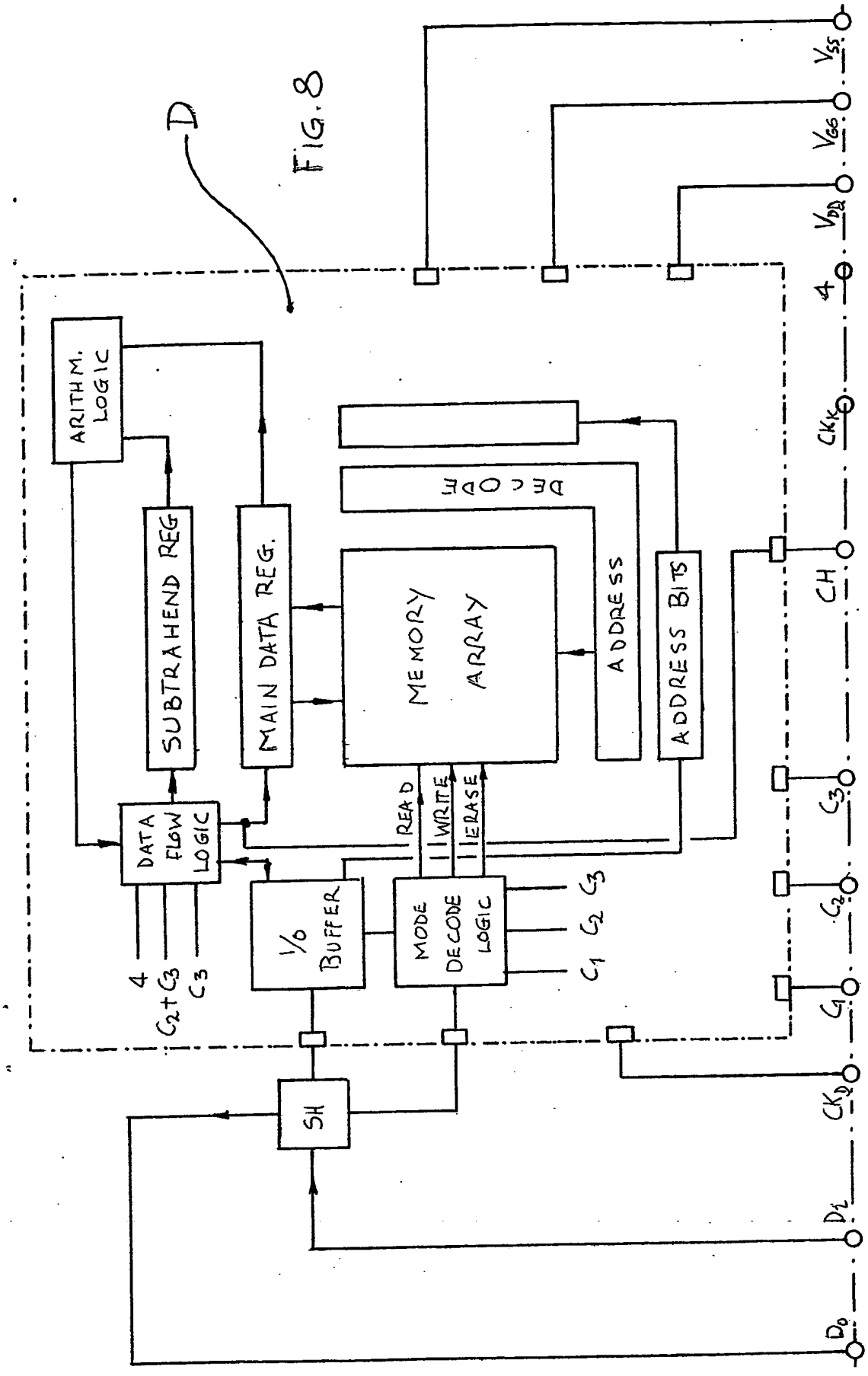
FIG. 8



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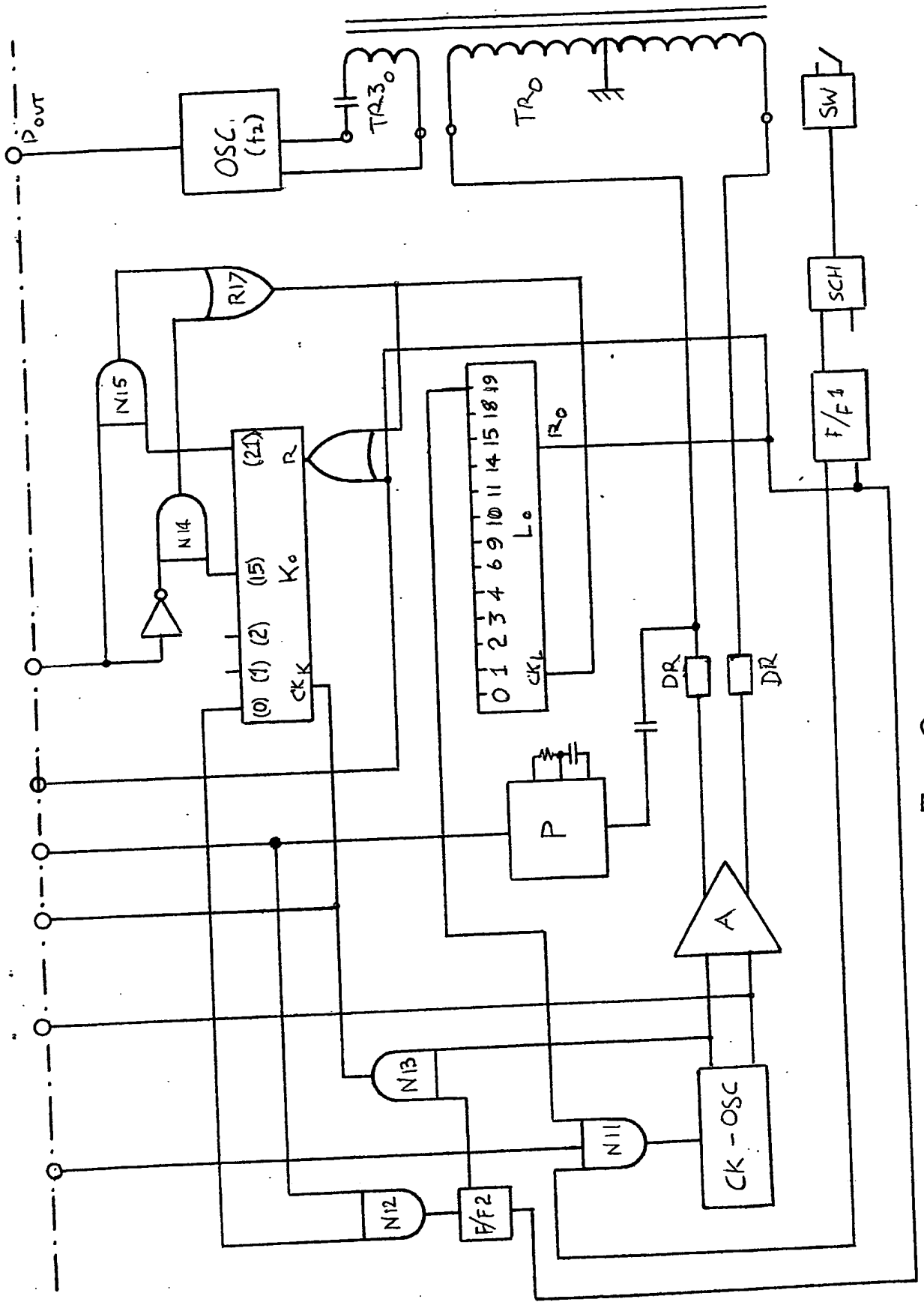

FIG 9

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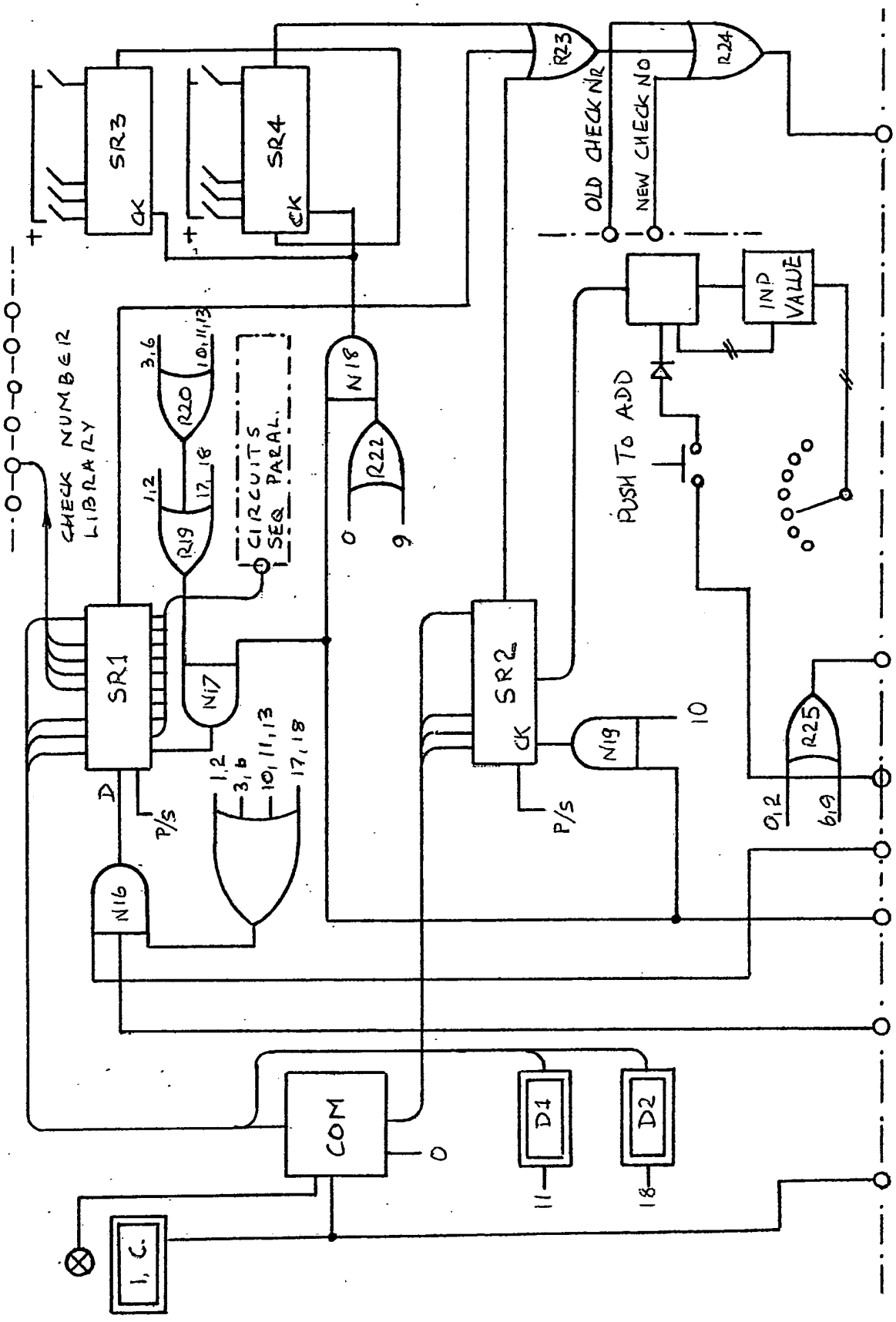

FIG 10.

SPECIFICATION

Solid state on-person data carrier

The principle of a solid state pocket-size carrier of electronically stored digital data and the manner of reactively transferring data bi-directionally between said carrier and a stationary computer has already been described by the applicants in a British patent.

One drawback of the initial design was the inadequate protection against accidental or fraudulent entry of new data. This would be particularly serious if the data carrier were used as a means of payment. Another drawback - when the data carrier contained variable data - was the dependence on a battery fitted into the data carrier.

This paper describes several innovative improvements. One of them is a method for battery-less operation. Another is a simplified and more robust mechanical construction of the data carrier. A third is the provision of protective data and a method for changing them at random intervals.

As to the first mentioned improvement it is characterized by the incorporation of an electrically alterable Memory chip. The second, by proposing a carrier structure which provides a single magnetic circuit instead of several such. The third improvement is achieved by the combination of dedicated hardware and software concepts.

In the drawing which illustrate these improvements,

Figure 1 is a partial cross section A - A through a portable data carrier

Figure 2 is a section B - B of the same

Figure 3 is a sectional view of the data sensor unit

Figure 4 is a section B - B through said data sensor showing drive and data coils

Figure 5 is an auxiliary sketch showing the chief electrical constitution of the current flow in the coils

Figures 6, 7 and *8* show the logic circuitry and associated power supply in the interior of the data carrier, Figure 1 and 2

Figures 9 and *10* show essential portions of the logic circuitry of the data processor and data transfer control unit which is associated with the data sensor unit, Figures 3 and 4.

Description of on-person data carrier

The same consists of a moulded or otherwise formed object 1 of ferric ceramic having a central core 1c and finlike extensions 1b. The corners 1a of the essentially square-like object are re-inforced in thickness. Coils 3 and 3a are fitted to the core. A further coil with much fewer number of turns than 3 is the coil 4. A printed circuit board 2 is attached to both sides of the central disk, and carries the various electrical and IC components such as flat packages 5 and 6 or capacitor 7, etc. The whole assembly may be closed by side plates 2a and potted in suitable resin or silicon compound. The finished ceramic component is the placed into two halves of a flat disk 10 the hollow spaces of which are filled with a softer grade of elastic material 9. Afterwards the two half spheres are moulded and fused together, for example by microwave heat.

Description of the Sensor Unit

The same consists in this example of two halves fitted into a supportive frame 12. This frame also serves as receptacle for the data carrier component 10, which, as the drawing indicates, may be dropped into the sensor unit where it comes to rest on piston 20. The latter may be so connected to mechanical actuators that on completion of the data transfer transaction it is either sideways withdrawn so that the carrier component is allowed to drop into a receptacle, or the piston 20 is lifted upwards to return the component (10) to the user. 13 and 14 are the two potlike parts. The outer diameter is about equal to the diagonal dimension of part 1 of the portable data component. Drive coils are 15 and 17; and 16 has again much fewer turns and mediates the data signal which in this proposal has a higher frequency that the clock pulses injected into coils 15 & 17.

Description of the circuitry of the on-person data carrier.

Figures 6, 7 and 8 should be laid together, with Figure 6 at the bottom and Figure 8 upmost to form one single circuit. The same provides an example for realizing an on-person data component by using an electrically alterable ROM. It is clear that the adaptation of the idea depends on the specific type of memory. The present description is oriented to a G I chip known as ER 1400 for which a data sheet is enclosed. This circuit depends on the use of separate erase pulses having a negative voltage for erasing a memory location. More recent devices may not require this operation step but, on the other hand, may require others. What is described hereunder should therefore be taken only as an illustration of a principle.

In the proposed Earom chip one modification has been made:

The General Instruments device uses all the combinations of three 'mode inputs' C_1 C_2 C_3 except C_1 plus C_2 plus C_3. In our setup, this combination is also used, namely for the command 'Enter data stream into the Subtrahent Register' (such subtrahent register is not provided in the General Instrument LSI.)

TR1 is identical with coil 3a in Figure 2, TR2 corresponds to coil 3, Figure 2, and TR3 corresponds to coil 4, Figure 2. TR1 carries clock pulses as indicated in Figure 5 and produces a d.c. output at V_{DD}. TR2 carries the same clock pulses and produces a negative d.c. voltage V_{GG}. TR3 carries only data pulses phase shifted

against the clock pulses as indicated in Figure 5. They consist of pulses of a much higher frequency which are detected by tuned circuits or by a phase locked loop circuit in the main control unit (figure 9). Clock pulses are shaped in unit E and passed on to Nandgate N9 and also to a combined rectifier and delay unit H. The same builds up a positive voltage level and provides a triggered-output to G only after a minimum voltage level is reached. G. is a bistable clock by output from E. When it goes high (which can only coincide with a rising clock-edge) Nandgate N9 goes low. At this time the zero condition still exists. However, And gate N3 produces an output because (o) count of counter K and inverter M1 have both high levels. This furnishes the OSC, unit (Figure 7) with a high enabling input via Or gate R16 and causes the phase-locked loop IC, P to respond to the frequency of the signal transferred from circuit Figure 6 to circuit figure 9. In consequence a pulse, - the so called synchronizing pulse - will be applied to gate N 12 (figure 9) and thus to F/F 2 bistable. From that moment onwards both systems, the portable data component and the data processing unit, are in readiness to accept count-down clock pulses originating at CK - OSC (figure 9). There are two counters in both systems, namely the L and K counter in the portable data component, and the L_o and K_o counter in the processor.

The K counters count up the word bits to be handled during each program step (in this example there are only two bit lengths, 15 and 2). The L counters count the program steps, and its decoded outputs are used for enabling such gates and functional units or sub-circuits as during a given program step must play a part.

The following are the program steps in this example:

K counter (0)	L counter 0	synchronizing pulse, one clock pulse wide
(1)-(20)	0	transfer value location address from processor unit to portable carrier
(1 - 14)	1	transfer value number from P.C. (portable carrier) to PR (processor).
(0)	1	compare in PR value number with debit number in COMP circuit, Fig.
(1 - 20)	2	address for the check word is transferred from PR to PC
	3	transfer the check number selected in the PR on the basis of library numbers to the PC and enter into the Subtrahent register
	4	Read out the check number from the addressed location in the Memory and serially pass on to the 'Arithmetic Logic Unit' in chip circuit D which concurrently also circulates the contents of the subtrahent register through the 'Arithmetic Logic'. (Serial comparison). If the output is different from zero all further operation is stopped.

CLAIMS

1. A data transfer system comprising a portable solid-state on-person data carrier and a computer unit, the portable carrier incorporating an electrically alterable memory device and means for causing mode control inputs to be activated in the portable component in accordance with a pre-arranged schedule.
2. As in Claim 1 in which the electrically alterable memory device comprises also a subtrahent register and and arithmetic logic circuit in an integrated condition.
3. As in Claim 1 in which the Computer comprises means for deriving from the data of the portable component one of several check numbers and means for presenting said check numbers to the portable component for internal comparison
4. As in any of the foregoing claims, means in the data carrying component for comparing check data received with check number held and means for disabling the clock circuit if disparity.
5. As in 1) a portable component as shown in Figure 1 and 2
6. As in 1), a data sensor device, as shown in Figure 3 and 4
7. As in 1), means for changing the address location of check numbers and value numbers held in the

portable on-person data carrier.

New claims or amendments to claims filed on 14 May 1979
Superseded claims 1-7
New or amended claims:- 1-11

1. A data transfer system comprising a portable solid-state on-person data carrier, a sensor unit interfacing data, and a computer unit, the portable data carrier incorporating an electrically alterable memory device and means for causing mode control inputs to be activated in the portable data carrier for consecutively arranged operations in accordance with a set schedule.

2. A data transfer system comprising a portable solid-state on-person data carrier, a sensor unit intercacing data, and a computer unit as in claim 1 in which the electrically alterable memory device comprises also a subtrahent register in an integrated condition.

3. A data transfer system as in claim 1 in which the computer unit comprises means for deriving from the data transmitted from the portable on-person data carrier an indication which one of a number of possible check numbers is stored in the said portable data carrier, and means for activating the register holding said number in order to transmit it to the said portable data carrier for comparison.

4. A data transfer system as in any of the foregoing claims in which said the data carrier contains means for internally comparing the check number received into its register with the check number held in one of its memory locations, and further means for disabling the continuation of the program if disparity of the two numbers is established.

5. A data transfer system as in Claim 4 in which the circuit of the said portable data component also comprises means for signalling to the computer unit any disparity between the said two numbers in such a manner that thereby no conclusions can be drawn as to the true check number held in one of the memory locations of the said portable data component.

6. A data transfer system comprising a portable On-person solid state data carrier, a sensor unit interfacing data and clock pulses, and a computer unit, in which the said data carrier consists of a twin shallow disk with flanged rim made of magnetically permeable material the bottom plate of which is common to both, each having a centrally disposed stud of same material (the studs pointing in opposite directions) the rims of the dishes and the centre studs serving as transformer yokes for two magnetic circuits which are completed by suitably shaped magnetic circuits when the said data carrier is placed into the said sensor unit.

7. A data transfer system comprising a portable on-person solid state data carrier, a sensor unit for data interfacing and clock pulses, and a computer unit as claimed in (6) in which the hollow spaces of the two dish-like parts are filled with electronic circuitry including large scale integrated elements, suitably sealed against intrusion of moisture or gases.

8. A data transfer system as in claims 1, 6 and 7 in which the computer unit provides unidirectional time reference signals (clock pulses) and electrical power to the said data component and exchanges bi-directionally data with the said portable data component whereby the said two magnetic circuits in the absence of data convey clock pulses having a definite phase relationship with each other, one of which is used as the time reference signal while both are used for powering the portable component.

9. A system as claimed in (8), in which data are transferred by associating a data bit with a phase change between the two pulse channels.

10. A data transfer system as in claims 1 and 6 comprising means for representing a data bit by a burst of high frequency oscillation superimposed on the clock pulse flow in at least one of the said two pulse channels.

11. A data transfer system as in claims 6 and 7, in which the portable data carrying component is enshrouded by a disk of resilient but formstable material to procure maximum protection against physical and temperature shocks.

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